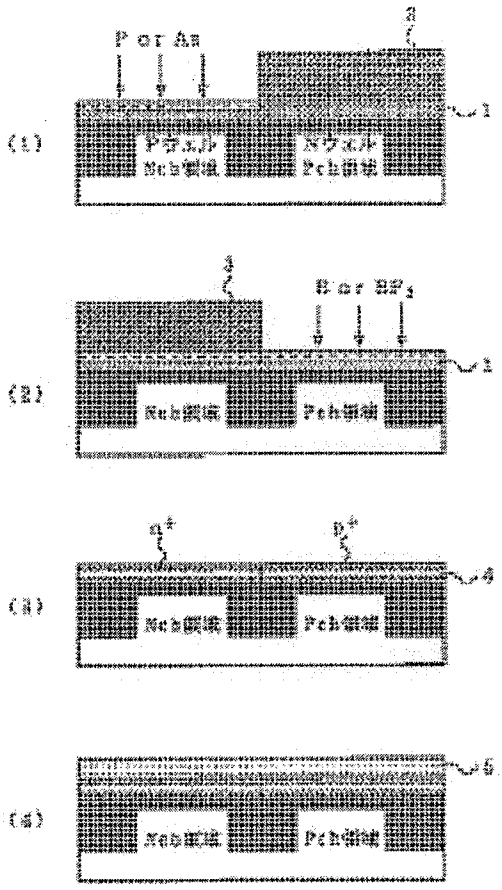
MANUFACTURE OF SEMICONDUCTOR DEVICE

Publication number: JP2000277626 (A)
Publication date: 2000-10-06
Inventor(s): ITO HIROSHI
Applicant(s): NIPPON ELECTRIC CO
Classification:
- international: ***H01L29/78; H01L21/265; H01L21/28; H01L21/8238; H01L27/092;*** **H01L29/66; H01L21/02; H01L21/70; H01L27/085;** (IPC1-7): H01L21/8238; H01L21/265; H01L21/28; H01L27/092; H01L29/78
- European:
Application number: JP19990079379 19990324
Priority number(s): JP19990079379 19990324

Also published as:
JP3277912 (B2)

Abstract of **JP 2000277626 (A)**

PROBLEM TO BE SOLVED: To simultaneously prevent generation of a depletion layer below a gate electrode and channeling when ions are implanted. SOLUTION: After a first amorphous silicon film 1 for a gate electrode is grown on a gate oxide film, ions are implanted in order to form N+ type and P+ type layers. A gate electrode is formed by growing a second amorphous silicon film 5 on the first amorphous silicon film. The second amorphous silicon film 5 is grown after heat treatment after ion implantation, in the case that the first amorphous silicon film 1 is thin for the purpose of silicide.

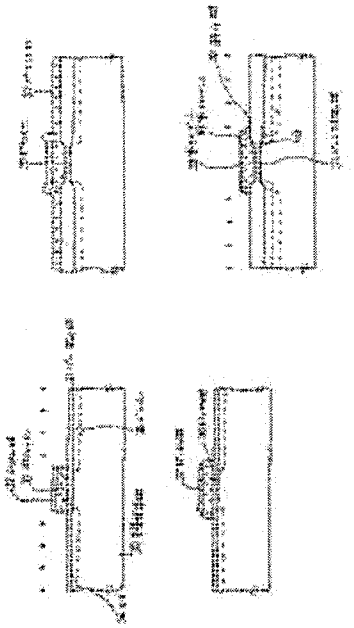


SEMICONDUCTOR DEVICE AND MANUFACTURE

Publication number: JP4112544 (A)
Publication date: 1992-04-14
Inventor(s): MATSUDA JUNICHI
Applicant(s): SANYO ELECTRIC CO
Classification:
- international: ***H01L29/78; H01L21/336;*** **H01L29/66; H01L21/02;** (IPC1-7): H01L21/336; H01L29/784
- European:
Application number: JP19900231685 19900831
Priority number(s): JP19900231685 19900831

Abstract of **JP 4112544 (A)**

PURPOSE:To reduce a generated capacity, and to reduce a tunneling current flowing between a high concentration drain and a substrate by forming a LO COS oxide film on the periphery of a first gate and the outside from the periphery, and forming a thick insulating film on low concentration source and drain. CONSTITUTION:A first gate 33, low concentration source 34, drain 35 are formed on a semiconductor substrate 30. Then, after a sidewall 36 is formed, a LOCOS oxidation is performed, and Si3N4 films 32, 36 used as antioxidation films are removed by hot phosphoric acid. Then, it is covered with a second polysilicon 37, and phosphorus is doped. Further, the polysilicon 37 is etched, and a second gate 38 is formed in a sidewall spacer shape. Here, the gates 33, 38 are electrically coupled, operated as the gates of a semiconductor device, and an oxide film 39 is formed on the gate surface. Thus, capacities generated in the low concentration source, drain, gate and oxide film can be reduced, and a tunneling current flowing between the high concentration drain and the substrate can be reduced.



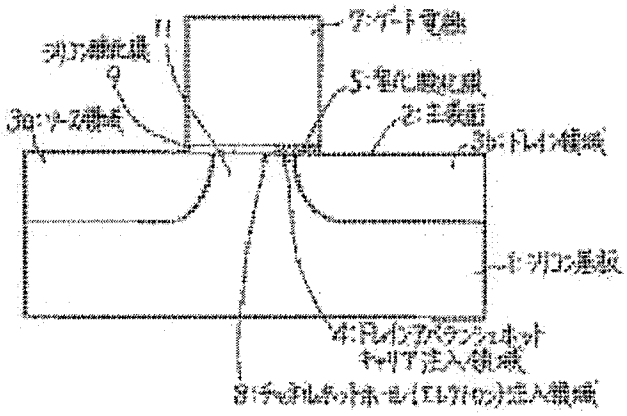
FIELD-EFFECT TRANSISTOR AND MANUFACTURING METHOD THEREOF

Publication number: JP5211330 (A)
Publication date: 1993-08-20
Inventor(s): KUSUNOKI SHIGERU; INUISHI MASAHIDE
Applicant(s): MITSUBISHI ELECTRIC CORP
Classification:
- international: ***H01L21/266; H01L21/28; H01L21/314; H01L21/336; H01L29/51; H01L29/78; H01L29/786;*** **H01L21/02; H01L29/40; H01L29/66;** (IPC1-7): H01L21/336; H01L29/784
- European: H01L21/28E2C2C; H01L21/266; H01L21/28E2C2N; H01L21/28E2C2V; H01L21/314B1; H01L21/336H1L; H01L21/336W; H01L29/51B1; H01L29/51N; H01L29/78; H01L29/78F4; H01L29/786B4B
Application number: JP19920176873 19920703
Priority number(s): JP19920176873 19920703; JP19910225686 19910905; JP19910323239 19911206

Also published as:
JP2652108 (B2)
DE4229574 (A1)
DE4229574 (C2)
US5369297 (A)
KR970000536 (B1)

Abstract of **JP 5211330 (A)**

PURPOSE:To provide the title field-effect transistor resistant to hot carrier and having powerful current drive force even if it is used at low a gate voltage. CONSTITUTION:A nitride oxide film 5 is formed in a drain avalanche hot carrier implanted region 4. This nitride oxide film 5 is more resistant to the drain avalanche hot carrier than a silicon oxide film 9. This silicon oxide film 9 formed on a channel hot electron implanted region 8 is more resistant to the channel hot electrons than the nitride oxide 5, furthermore having the more powerful current drive force at a low gate voltage than the nitride oxide film 5.

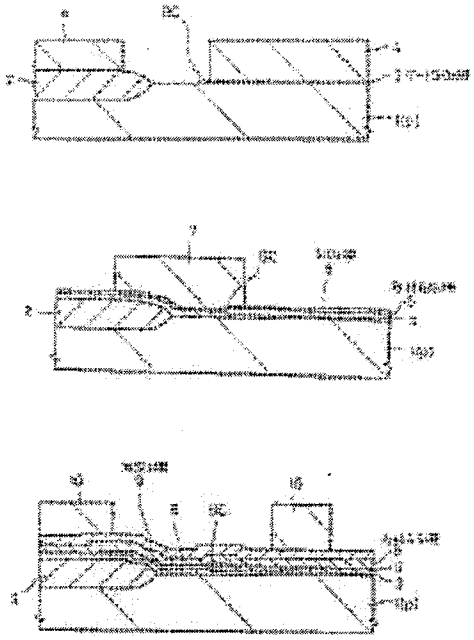


MANUFACTURE OF SEMICONDUCTOR DEVICE

Publication number: JP4010620 (A)
Publication date: 1992-01-14
Inventor(s): KAYAMA SHIGEKI
Applicant(s): SONY CORP
Classification:
- international: ***H01L29/78; H01L21/28; H01L21/336;*** **H01L29/66; H01L21/02;** (IPC1-7): H01L21/28
- European:
Application number: JP19900114736 19900427
Priority number(s): JP19900114736 19900427

Abstract of **JP 4010620 (A)**

PURPOSE:To prevent a semiconductor substrate exposed at a buried contact section from being etched, at time of etching for forming a gate electrode, by forming an etching stopper film on the first conductor film so as to lap over at least a gate insulating film. CONSTITUTION:After a resist pattern 4 is removed and a polycrystalline Si film 5 is formed on the whole surface, impurities such as phosphorus (P) are doped into this polycrystalline Si film 5. And an SiO2 film 6 as an etching stopper is formed on the surface of the polycrystalline Si film 5. After that, a resist pattern 7 in a specified shape is formed on this SiO2 film 6 so as to cover the surface of a buried contact section completely. Then, by etching the SiO2 film 6 using this resist pattern 7 as a mask, the SiO2 film 6 is left at the part of a contact hole BC for a buried contact and at a part in its vicin ity so as to lap over the gate SiO2 film 5. Next, after a polycrystalline Si film 8 is formed on the whole surface and impurities such as P are doped into this polycrystalline Si film 8, a WSix film 9 is formed on this polycrystalline Si film 8.



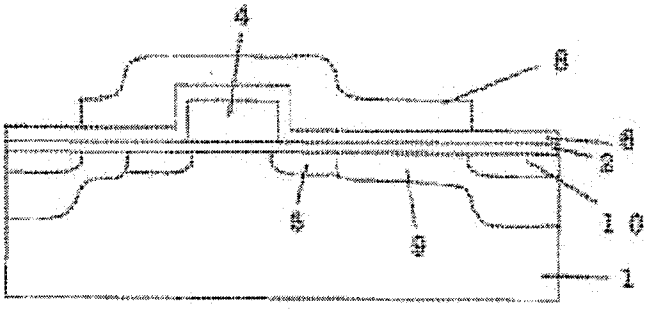
SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Publication number: JP2002164536 (A)
Publication date: 2002-06-07
Inventor(s): AOKI HITOSHI
Applicant(s): SHARP KK
Classification:
- international: ***H01L21/8247; H01L21/336; H01L21/8234; H01L21/8238; H01L27/088; H01L27/092; H01L27/115; H01L29/423; H01L29/78; H01L29/786; H01L29/788; H01L29/792;*** *H01L27/12;* **H01L21/02; H01L21/70; H01L27/085; H01L27/115; H01L29/40; H01L29/66;** H01L27/12; (IPC1-7): H01L29/78; H01L21/8238; H01L21/8247; H01L27/092; H01L27/115; H01L29/786; H01L29/788; H01L29/792
- European: H01L21/336H4; H01L29/423D2B2; H01L29/78F3
Application number: JP20000359535 20001127
Priority number(s): JP20000359535 20001127

Also published as:
JP3594550 (B2)
US2002072173 (A1)
US6888191 (B2)
TW284984 (B)
KR20020041282 (A)

Abstract of **JP 2002164536 (A)**

PROBLEM TO BE SOLVED: To provide a transistor with high dielectric strength which is suitable to a microprocess. SOLUTION: The semiconductor device is composed of a first electrode 4 which is formed on a semiconductor substrate 1 of a first conductive type across a gate insulating film 2, a second electrode 8 which is formed on at least the electrode 4 across an intermediate insulating film 6, and a couple of impurity regions of a second conductive type which are formed on the semiconductor substrate 1 separately from each other; and at least one of the impurity regions is formed of a lightly doped region 5, an intermediately doped region 9, and a heavily doped region 10 adjacently in order from the area side right below the first electrode 4.



SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

Publication number: JP11103050 (A)
Publication date: 1999-04-13
Inventor(s): NAGANUMA HIROYUKI; SUGAYA SHINJI
Applicant(s): FUJITSU LTD
Classification:
- international: ***H01L29/78; H01L21/28;*** *H01L21/316;* **H01L29/66; H01L21/02;** (IPC1-7): H01L29/78
- European: H01L21/28E2C2V; H01L21/28E2C2B
Application number: JP19970264410 19970929
Priority number(s): JP19970264410 19970929

Also published as:
US6277718 (B1)

Abstract of **JP 11103050 (A)**

PROBLEM TO BE SOLVED: To obtain a semiconductor device having stable electric characteristics, by forming an insulation film on a semiconductor substrate, introducing fluorine to the insulation film, then forming a semiconductor layer on the insulation film, and introducing impurities containing hydrogen to the semiconductor layer. SOLUTION: A gate insulation film 12 is formed on a silicon substrate 10 having a plane azimuth (100), a polysilicon layer 14 is deposited on the gate insulation film 12 by CVD method, and fluorine ion is implanted from the top of the polysilicon layer 14. Next, photo resist is applied to the top of the polysilicon layer 14, and exposure and developing are performed and patterning to the shape of gate electrode 16 is performed. Thereafter, a silicon oxide film is formed to the whole surface, its silicon oxide film is etched, and a side wall 18 is formed. In addition, by using the gate electrode 16 and the side wall 18 as a mask, decaborane is implanted to a source/drain diffusion layer 20, thereby producing a p-type surface channel type semiconductor device.